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PTO/SB/05 (2/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5258D
First Inventor or Application Identifier	Sanjay Dabral
Title	Diode and Transistor Design for High Speed I/O
Express Mail Label No.	EL635878821US

JC851 U.S. PTO 09/651385 08/29/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g. PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)
2. [X] Specification Total Pages 30
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C.113)* Total Sheets 8
4. Oath or Declaration Total Pages 3
   a. [ ] Newly executed (original copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
(when there is an assignee)
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ] Other: . . . . . .

16. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 107,351

Prior application Information: Examiner Ortiz, E. Group/Art Unit: 2815

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number of Bar Code Label* *(Insert Customer No. or Attach bare code label here)* or [X] *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
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Name (Print/Type)	William Thomas Babbitt, Reg. No. 39,591		
Signature	William T Babbitt	Date	8/29/00

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

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FEE TRANSMITTAL

Petent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported be a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§ 1.28 and 1 28

TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known	
Application Number	
Filing Date	08/29/00
First Named Inventor	Sanjay Dabral, et al.
Examiner Name	Ortiz, E.
Group Art Unit	2815
Attorney Docket Number	042390.P5258D

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

2. ☒ Payment Enclosed:

☒ Check ☐ Money Order ☐ Other

FEE CALCULATION (fees effective 10/01/96)

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	$690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims 10	-20** = 0	X	$18.00	=	0.00
Independent Claims 1	-3** = 0	X	$78.00	=	0.00
Multiple Dependent				=	

***or number of previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	270	204	135	Multiple Dependent claim
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,360	138	1,360	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidably	
141	1,210	241	605	Petition to revive - unintentionally	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	William Thomas Babbitt, Reg. No. 39,591			Reg. Number	
Signature	William T Babbitt	Date	8/29/00	Deposit Account User ID	02-2666

Attorney's Docket No. 042390.P5258D
Express Mail No. EL635878210US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sanjay Dabral and Krishna Seshan

Serial No.

Filed: August 29, 2000

For: *DIODE AND TRANSISTOR DESIGN FOR HIGH SPEED I/O*

Divisional Application of:
Serial No. 09/107,351
Filed: June 30, 1998

Examiner: Ortiz, E.

Art Unit 2815

PRELIMINARY AMENDMENT

Box New Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In connection with the filing of the Divisional Application under Rule 1.53(b), Applicants respectfully request entry of the following amendment.

Please cancel claims 1-19.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: 8/29/00

William Thomas Babbitt, Reg. No. 39,591

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Our File No: 042390.P5258
Express Mail No: EM560821449US

UNITED STATES LETTERS PATENT APPLICATION

FOR

DIODE AND TRANSISTOR DESIGN FOR HIGH SPEED I/O

Inventors: Sanjay Dabral
Krishna Seshan

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuit devices and more particularly to layout techniques for such devices.

Description of Related Art

One area where parasitic capacitance is noted is in input/output (I/O) buffer circuits. For high speed I/O circuits, the parasitic capacitance is one limiter to the fast transitioning edges of the circuit. The larger the capacitance, the slower the charging or discharging, resulting in degraded bus performance. Thus, many efforts have been put forth to reduce the capacitive load and create faster transitions which in turn leads to faster I/O circuits.

The input signals to an integrated circuit, for example, a metal oxide semiconductor (MOS) integrated circuit, are generally fed to transistors. If the voltage applied to the transistor becomes excessive, the gate oxide can break down, the junctions can be destroyed, and the metal to the transistor can be destroyed. Excessive voltages are voltages in excess of the normal operating voltages of the circuit. For example, voltages far in excess of the nominal operating voltage of an integrated circuit, may be impressed upon the inputs to the circuit during either human-operator or mechanical handling operations.

The main source of excessive high voltages to integrated circuits is triboelectricity. Triboelectricity is caused when two

materials are rubbed together. A common situation is a person developing very high static voltage (i.e., a few hundred to a few thousand volts) simply by walking across a room or by removing an integrated circuit from its plastic package, even when careful handling procedures are followed. If such a high voltage is applied to the pins of an integrated circuit package, its discharge, referred to as ElectroStatic Discharge (ESD), can cause breakdown of the devices to which the voltage is applied. The breakdown event may cause sufficient damage to produce immediate destruction of the integrated circuit, or it may weaken the device enough that it will fail early in the operating life of the integrated circuit.

In general, all inputs (e.g., pins) of MOS integrated circuits are provided with protection circuits to prevent excessive voltages from damaging the MOS transistors. These protection circuits are normally placed at the input and output pads on a chip and the transistor gates to which the pads are connected. The protection circuits are designed to begin conducting or to undergo breakdown, thereby providing an electrical path to ground (or to the power-supply rail), in the presence of excessive voltages, generally ESD. Since the breakdown mechanism is designed to be non-destructive, the circuits provide a normally open path that closes only when a high voltage appears at the input or output terminals, harmlessly discharging the node to which it is connected.

Typically, two types of protection circuits are used to provide protection against ESD damage: Diode breakdown and diode

conduction. Diode protection is obtained by using the diode-breakdown or diode-conduction phenomenon to provide an electrical path in the semiconductor, e.g., silicon, substrate that consists of a diffused diode region of a doping type opposite to that of the substrate (for example, p-type and n-type doping, respectively). This diffused region is connected between the input pad and substrate. If a reverse-bias voltage greater than the breakdown voltage of the resultant pn junction is applied, the diffusion region (which otherwise works as a diode) undergoes breakdown. Furthermore, the diffused region will also clamp a negative-going ESD transition at the chip input to one diode drop below the substrate voltage. In CMOS technologies, an additional protection diode can be added by utilizing the pn junction that exists between a p-type region and the body region of the PMOS device (an n-type region that is connected to V_{CC}). This diode is utilized as a protection device when a connection is made between the pad and a p-type region. This diode will generally clamp positive-going transitions to one diode drop above V_{CC} (V_{CC} is generally OV during ESD).

Figure 1 shows a known input/output (I/O) buffer circuit 10 having ESD protection components, diodes D1 and D2. CMOS I/O buffer circuit 10 includes PMOS device 20 coupled to NMOS devices 30. The devices of circuit 10 are connected to I/O pad 40. Between pad 40 and the devices is a negative zap protection diode D1. Between I/O pad 40 and PMOS circuit 20 is forward-biased protection diode D2.

Figure 2 shows a prior art layout of a portion of I/O buffer circuit 10 of **Figure 1**, specifically illustrating the layout of PMOS device 20 and ESD protection diode D2. **Figure 2** shows PMOS field effect transistor (MOSFET) device 20 made up of polysilicon gate 60 separating source region 65 and drain region 70 with individual contacts 72 and 75 to source and drain regions 65 and 70, respectively. In this embodiment, PMOS device 20 is in an n-well with p-type (p^+ doped) source and drain regions 65 and 70, respectively. **Figure 2** also shows conventional PMOS diode D2 adjacent drain 70 of PMOS device 20. In **Figure 2**, p-type area 70 acts as both a MOSFET drain 70 and the D2 diode anode. Adjacent drain/anode 70 is an n-type (n^+-doped) cathode region 80 in the n-well.

The critical size of a protection circuit and of a performance circuit are independent of one another. For example, protection diodes D1 and D2 are sized (i.e., a specific volume of semiconductor material allocated) in accordance with the amount of charge that is contemplated to be dissipated. If the power is dissipated into too small a volume of silicon, the silicon can be heated beyond its melting point and the device destroyed. Transistor devices 20 and 30 are likewise sized, for example, in accordance with the voltage drive capabilities of the output driver.

In typical prior art structures, such as the I/O scheme illustrated in **Figures 1** and **2**, the size of PMOS protection D2 diode corresponds to the size of the PMOS device because they share a common junction (drain or anode). To accommodate layout

concerns and processing conveniences, D2 diode is integrated with PMOS device 20. In other words, the critical size of either D2 diode or PMOS device 20 determines the size of the corresponding device. If D2 diode size is critical and controls, PMOS device 20 size is enlarged to accommodate the large diode. If, on the other hand, PMOS device 20 is critical and controls, D2 diode size is enlarged beyond what is necessary for an ESD protection circuit. It is to be appreciated that techniques for determining a critical diode size for addressing ESD concerns are well known and, so as not to obscure the invention, will not be discussed herein. For purposes of the invention, it is necessary to understand only that there is a critical, scaleable minimum size, for example, a minimum sized D2 diode, that will protect a performance circuit, such as a PMOS device or NMOS device, from ESD damage. Similarly, it is well known in the art how to size performance circuits, such as PMOS drivers. Accordingly, techniques for sizing performance circuits will not be presented herein.

I/O circuit 10 pad capacitance has several elements, including the NMOS device, the PMOS device, the wire bond or C4 pad, the pad to V_{CCP} diode (D2) and the V_{SS} to pad diode (D1). The diffusion capacitance is high because it is a p^+-type diffusion in an n-type well. As noted above, the typical PMOS device 20 of an I/O circuit includes a D2 diode, where one edge of the p-type drain serves as the drain and the other as the diode anode or edge. This sharing makes the diode scale up or down with PMOS device 20 size. For example, in a mixed voltage environment, when a high voltage technology wants to drive a low voltage I/O,

PMOS device 20 size can be very large. Therefore, D2 diode size is much larger than required resulting in extra capacitive loading.

On the other hand, there are also performance circuits that do not need a large PMOS pull-up device. One example is an open drain buffer. To meet the minimum diode size requirement, however, the PMOS size is increased (and generally tied off).

Increasing the size of either the MOSFET device or the ESD protection circuit, e.g., diode, directly leads to increased capacitance. In general, the size of a device (e.g., area, volume, etc.) is directly related to its parasitic capacitance. Thus, what is needed is a layout, particularly an I/O layout, that minimizes parasitic capacitance contributed by the performance and protection circuits without sacrificing the required actions of either circuit.

SUMMARY OF THE INVENTION

An integrated circuit is disclosed. The integrated circuit includes a performance circuit occupying a first area of an integrated circuit substrate and a protection circuit coupled to the performance circuit commensurate with dissipating an amount of predetermined charge incident on the performance circuit and occupying a second area of an integrated circuit substrate separate from the first area.

Additional features and benefits of the invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a typical I/O scheme having ESD protection components.

Figure 2 shows a circuit layout of an ESD diode integrated with a PMOS device with a shared p-type area acting as a MOSFET drain and a diode anode.

Figure 3 schematically illustrates the layout of a PMOS device partitioned from its ESD protection diode in accordance with an embodiment of the invention.

Figure 4 schematically illustrates the layout of one embodiment of the diode portion of a partitioned integrated circuit in accordance with the invention.

Figure 5 schematically illustrates a cross-sectional side view of the diode through line A-A of **Figure 4** in accordance with an embodiment of the invention.

Figure 6 schematically illustrates a layout of a second embodiment of the diode portion of a partitioned integrated circuit in accordance with the invention wherein the ratio of the periphery to the area of the anode is increased.

Figure 7 schematically illustrates an individual p-type anode of **Figure 6** and shows the distribution of current through the anode in accordance with the embodiment of the invention.

Figure 8 schematically illustrates a layout of a third embodiment of the diode portion of a partitioned integrated circuit in accordance with an embodiment of the invention wherein an n-type area faces each facet of individual p-type anodes.

Figure 9 schematically illustrates a single p-type anode of **Figure 8** and illustrates the current spreading for this type of structure in accordance with an embodiment of the invention.

Figure 10(a) schematically illustrates a layout of a prior art anode stripe having contacts removed from viable areas for unit cells of the anode.

Figure 10(b) schematically illustrates a layout of an improved anode design in accordance with an embodiment of the invention showing a maximization of periphery in a given area.

Figure 11 schematically illustrates a layout of an embodiment of a performance circuit of a partitioned integrated circuit in accordance with the invention.

Figure 12 schematically illustrates a layout of a second embodiment of a performance circuit of a partitioned integrated circuit in accordance with the invention.

Figure 13 schematically illustrates a top view of a layout of a portion of an integrated circuit chip showing ladder type I/O circuits at a corner.

Figure 14 schematically illustrates a top view of a layout of a portion of an integrated circuit chip showing waffle type I/O circuits at a corner.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to an integrated circuit and a method of forming an integrated circuit having a performance circuit occupying a first area of an integrated circuit substrate, and a protection circuit coupled to the performance circuit and occupying a second area of the integrated circuit substrate separate from the first area. The partitioning of the performance circuit and protection circuit is scaleable to different device circuit requirements and may be utilized wherever a protection circuit is used to prevent ESD from causing breakdown of integrated circuit devices. The partitioned performance circuit and protection circuit can be utilized in I/O circuits with the objective of maximizing the protection circuit current capability and minimizing the total capacitance at the I/O circuit pad.

The following detailed description describes an improved circuit and a method of forming an improved circuit such as an I/O unit similar to the circuits described with reference to **Figures 2**, **1(a)**, and **1(b)** and the accompanying text. More particularly, the following description relates to a PMOS device and the D2 ESD diode protection circuit for the PMOS device. It is to be appreciated, however, that the invention is not to be limited to I/O circuits or more specifically to PMOS/ESD circuits or CMOS performance circuits and diode protection circuits. Instead, the invention will apply anywhere ESD protection circuits are implemented and the objective is to increase the current

capability of the protection circuit and decrease the capacitance of the performance circuit.

Figure 3 illustrates an embodiment of the invention where the ESD protection circuit is partitioned from the performance circuit. In this example, the performance circuit is, for example, PMOS device 110 of a CMOS I/O circuit in an n-well. ESD protection circuit is, for example, D2 diode 115.

As illustrated in **Figure 3**, the invention contemplates that the protection circuit, such as for example, ESD diode 115, is separate from the performance circuit, in this case PMOS device 110 in terms of area or volume utilization of a semiconductor substrate. In the case of D2 diode 115, D2 diode 115 is partitioned from PMOS device 110. The drain region of PMOS device 110 and the anode of D2 diode 115 are not formed of a common doped area of the substrate, such as was described in **Figure 2** and the accompanying text.

The partitioning of D2 diode 115 from PMOS device 110 ensures the best utilization of integrated circuit space. The partitioning allows PMOS device 110 to be scaled up or down while maintaining D2 diode 115 at, for example, the ESD critical size. The partitioning reduces the capacitance (due to the reduction in excess area of either D2 diode 115 or PMOS device 110) while retaining the ESD current handling capability over a standard PMOS driver and ESD protection D2 diode 115. The reduction in capacitance leads to faster transition times, enhancing bus speed. In addition, correctly sized and improved protection circuits (e.g., ESD diodes) and performance circuits (e.g., PMOS drivers)

result in an on-chip area reduction when compared to prior art devices.

Comparisons have been made between the partitioned performance/protection circuits and prior art coupled circuits. In one embodiment, a partitioned bimodal driver having a large PMOS device yields an estimated 22% gain in capacitance reduction over a prior art driver coupled bimodal driver. In that same embodiment, the partitioned driver decreases the area for both the performance circuit and protection circuit by an estimated 22%. If a D2 diode size equal to that of an input buffer (e.g., input D2 diode) is used in the output (PMOS) section, the capacitance will see an estimated 36% capacitance reduction gain, and a 37% area reduction.

The above discussion illustrates how the capacitance and required area of an I/O driver with protection circuits are reduced by de-coupling or partitioning the protection circuit from the performance circuit. In addition to this reduction, the invention also contemplates that, in the case of a D2 diode, in particular, the current discharge capability of a diode can be enhanced. This allows a smaller diode to be used while maintaining the critical current discharging requirements necessary for an ESD protection circuit.

Figure 4 illustrates a layout of partitioned D2 diode 115. Partitioned D2 diode 115 is formed, for example, in an n-type well 120 with n-type doped area regions 125 and 145 serving as cathodes adjacent a p-type doped region 135 anode. Contacts 130 are made to n-type area regions 125 and 145 to, for example,

dissipate any charge to a suitable power supply. Similarly, contacts 140 are made to p-type region 135 to, for example, link the diode to the performance circuit. **Figure 4** shows p-type area 135 illustratively represented as a plurality of unit cells, each unit cell represented by a contact 130 to the p-type area 135. A unit cell is the minimum area necessary to place a contact in a minimum area, e.g., a minimum p-type area. **Figure 5** shows a cross-sectional side view taken through line A-A of **Figure 4**. This formation of unit cells of lateral stripes 125 and 145 adjacent lateral stripe 135 is referred to herein as a "striped" design.

As illustrated by the arrows in **Figure 4**, when ESD diode 115 discharges an ESD current, the current travels laterally (as indicated by the arrows) toward two edges of each p-type unit cell of an area 135. In diode conduction, the periphery or edges of the unit cell contribute more to current dissipation than the area. Thus, the periphery to area ratio as a measurement of p-type each unit cell of area 135 to dissipate charge toward the cathode is limited to two edges of each unit, i.e., 2/4 or 1/2 of the periphery of each unit cell is available.

The invention contemplates, that in addition to the structure shown in **Figures 4** and **5**, the p-type unit cells of the diode may be made as islands. **Figure 6** shows one such island configuration. In **Figure 6**, unit cells 122 of p-type doped area region 135 are formed in n-well 120 and are located adjacent stripes of n-type regions 125 and 145. Each unit cell 122 contains a contact 130. This formation of unit cell 122 adjacent

lateral stripes 135 is referred to herein as an "island" design. **Figure 7** illustrates a top view of a single unit cell 122 taken from the diode layout of **Figure 6**. Unit cell 122 sits in n-well region 120 separated from stripes of n-type regions 125 and 145 adjacent to the opposing sides of unit cell 122. In this manner, current paths forming along unit cell 122 sides substantially parallel to n-type stripes 125 and 145 have a direct path toward the n-type stripes, much like the prior art diode structures. In addition, since the edges of unit cell 122 that are orthogonal or substantially perpendicular to stripes 125 and 145 are adjacent n-well 120, current 150 can travel through these edges toward stripes 125 and 145 improving the discharge capability of unit cell 122 over the unit cells described with reference to **Figures 4** and **5**. As can be seen in **Figure 7**, by creating unit cell 122 as an island, the p-type area region can dissipate charge in four directions.

In the condition where the p-type/n-well diode is strongly forward biased, on the order of 0.8V, a conductivity modulation occurs in n-well 120. During conductivity modulation, there is sufficient hole injection into n-well 120 that even the electrons in n-well 120 exceed the doping density (electrons increase to maintain charge neutrality). Thus, the resistivity of n-well 120 falls dramatically at high conduction, thereby allowing all sides of unit cell 122 to conduct almost uniformly. In such cases, from a geometrical consideration, each unit cell 122 has at least four times the advantage over a diode shared as a drain as in prior art structures (**Figure 2** and the accompanying text), or

twice the advantage over a striped diode using both edges as described with reference to the embodiment of the invention described in **Figures 4** and **5** and the accompanying text.

If higher current uniformity is desired, **Figures 8** and **9** illustrate a third embodiment of the partitioned protection circuit of the invention. In **Figure 8**, unit cells 133 of p-type doped regions 133 are formed in n-well 120. p-type regions 160 are formed adjacent each edge of p-type units 133. In this manner, each unit cell 133 becomes an island in n-well 120 surrounded by n-type region 160. This surrounding of unit cell 133 with n-type region 160 is referred to herein as a "waffle" design.

Figure 9 shows the current paths 165 from an edge of one unit cell 133 of **Figure 8**. The current spreading improves the diode resistance over prior art diode structures. Resistance can be estimated and compared based on the length of the current path. Current path 165 has a trapezoidal shape, and the effective width of the path can be estimated as the average of the widths of the current source and sink. In **Figure 9**, the current source has width "3S" and sink width "5S." The diode resistance is reduced by current spreading, spreading a distance "4S." Therefore, the resistive improvement with respect to a linear diode stripe implementation is about "1S/3S", or 33%.

A comparison between a prior art coupled bimodal driver and an embodiment of a decoupled bimodal driver with improved unit cell diode design of the invention has been made. The decoupling and improved unit cell diode reduces the capacitance of the

bimodal driver by an estimated 34% and reduces the area by an estimated 27% for the waffle diode configuration of the invention compared to the integrated diode of the prior art.

Comparing the island diode presented in **Figures 6** and **7** to the waffle diode presented in **Figures 8** and **9**, one estimate is that the waffle diode occupies approximately half the area of the striped diode with other factors remaining the same. The capacitance savings is calculated at about 34%.

The prior art has reported enhanced conduction at the corners of a unit cell of, for example, an anode area stripe such as described with reference to **Figure 2** and the accompanying text. In S.H. Voldman, V.P. Gross, M.J. Hargrove, J.M. Never, J.A. Slinkman, M.P. O'Boyle, T.S. Scott, J.D. Deleckl, "Shallow Trench Isolation Double Diode Electrostatic Discharge Circuit and Interaction With DRAM Output Circuits," Proc. EOS/ESD Symp. 1992, at page 277, and S.H. Voldman, "ESD Protection In A Mixed Voltage Interface and Multirail Disconnected Power Grid Environment in 0.5 μm and 0.25 μm Channel Length CMOS Technology," Proc. EOS/ESD Simp., 1994 at 253, the authors report up to 56% higher currents were observed at the ends or corners compared to a length edge of a diode. In those cases, the enhanced conduction at the corner led to diode destruction, because of uneven current sharing between the length edge and the corners leading to higher temperature at the corners. This enhanced conduction was explained as a three-dimensional implant effect where the junction at the corner becomes cylindrical, as opposed to planar over a straight edge for a trench isolated technology. For a Local

Oxidation of Silicon (LOCOS) technology, the junction shapes are spherical at the corner and cylindrical at the straight edge).

The solution to the problem proposed by the prior art was to eliminate the unit cell at or near the corners, thus reducing the current conduction at the corners. This could be done, for example, by removing the contacts near the ends of, for example, an anode area stripe, as shown in **Figure 10(a)**. **Figure 10(a)** shows anode stripe 190 having unit cells 1902, 1903, and 1904. In areas 1901 and 1905, contacts are not placed and viable areas for unit cells are not utilized and a capacitance penalty is paid.

In contrast to the prior art teachings, particularly the teachings of Voldman, et al. noted above, the invention contemplates that the diode consists entirely of corners, with very short straight segments. This is shown in **Figure 10(b)** in the contrasting structure of anode area 195 in accordance with an embodiment of the invention. In **Figure 10(b)**, each unit cell 1951-1955 is a diode made up of a multitude (4) of only corners. Therefore, uneven current distribution will not occur. The overall diode performance will be biased toward the enhanced conduction mode and the "problem" recognized by the prior art of enhanced conduction is turned into a beneficial gain.

The p-type to n-well diode is a common ESD protection device employed in many input and input/output pads, including CMOS, mixed voltage, etc. By partitioning the diode and the I/O circuit, and also enhancing the current capability of the diode itself, the area of the semiconductor substrate is significantly

reduced and the capacitive load on an I/O pad and on a bus is significantly reduced. The reduction in the capacitive load enhances speed and, to a smaller degree, saves system power. The enhanced current capability of the island and waffle unit cell diodes also reduce the resistance which helps to protect the I/O circuit during an ESD occurrence. Similar area, capacitance, and resistance improvements can be achieved by applying similar principles to other performance/protection circuit, including, in this case, the V_{SS} to pad D1 diode. With regard to the D1 diode, for example, the partitioning and unit cell designs apply equally as well. In the case of implementing the D1 diode in a p-type epitaxial substrate, the D1 diode need not be in a well, but can be made simply by placing an n-type tap or region in the substrate and forming a contact to the tap. It is also to be appreciated that, although logic families conventionally use p-type epitaxial substrates, if another type of substrate, e.g., an n-type substrate, is used, the construction of the D1 and D2 diodes can be suitably adjusted.

Much of the above discussion has focused on optimizing the partitioned diode portion of an I/O circuit. In much the same way, the performance portion of the I/O circuit can similarly be enhanced. As shown in **Figure 2**, a prior art PMOS driver 20 utilizes one edge of drain 70 of a MOSFET for transistor action and the other for creating an ESD diode. Each contact 75 to drain region 70 to define a unit cell has a width W and a capacitance C.

Figure 11 shows a top view of a portion of the partitioned performance circuit in accordance with one embodiment

of the invention. **Figure 11** shows a PMOS device 250 in an n-well 220. PMOS device 250 includes polysilicon gate 260 between source region 235 and drain region 225. Adjacent drain region 225 opposite the edge adjacent source region 235 is second source region 260. Similarly, polysilicon gate 270 overlies a semiconductor substrate having p-type doped source region 235 and drain region 245. Adjacent the edge of drain region 245 opposite source region 235 is a second source region 255. Drain regions 225 and 245 are each divided into a plurality of unit cells, each unit cell having a contact 230 to drain region 225 and 245, respectively.

In the structure shown in **Figure 11**, the absence of an integrated protection allows the transistor devices to be scaled independent of the protection circuits, e.g., independent of the ESD protection diode. The absence of an integrated protection circuit such as a diode also allows both sides of drains 225 and 245 of respective PMOS transistor devices to be exploited. Thus, for each contact 230 to a unit cell of drain region 225 and 245, respectively, there is twice the width (2W) for a given capacitance C. Thus, a doubling of the width to capacitance ratio is obtained over the prior art structure shown in **Figure 2**.

Figure 12 shows a layout of a second embodiment of the performance portion of the partitioned integrated circuit of the invention. In **Figure 12**, individual unit cells 280 include a p-type doped region 285 and contact 290 in n-well 220. Here again, a unit cell is that minimum amount of p-typed doped area that will support a contact. Overlying and surrounding the periphery of

unit cell 280 is polysilicon gate 295. In this case, p-type doped regions 285 of unit cells 280 serve as drain regions for the PMOS FET device. Surrounding drain region 285 of unit cells 280 is p-type source region 310. Summarizing the unit cell 280 structure as a waffle structure, one drain contact 290 serves four sides. Accordingly, the width to capacitance ratio is 4W/C, a gain of four times the width to capacitance ratio over prior art structures such as described in **Figure 2** and the accompanying text.

The waffle transistors described above can be analytically or empirically modeled similar to prior art "Ladder" transistors such as shown in **Figure 2** and the accompanying text. For a right angle edged waffle MOSFET, the width is four times the inner width (assuming small gate lengths). If the corners are not sharp and a right triangle is placed at each corner, the effective width of the corners is diminished, such that the effective width is estimated by the known relationship:

$$\Delta W_{eff} = \frac{4L}{\pi} \ln \frac{LW_s}{L}$$

where W_S is the length of the triangle's side. Straight gate edges should be added to this number.

Another advantage of the waffle design of transistors is that asymmetries arising in I/O circuits due to chip layout are avoided. This occurs generally on the corners of a chip where ladder type devices of the prior art that were laid out in one direction changed direction at the corner, for example, going from vertical to horizontal. **Figure 13** shows the example of a ladder

type transistor layout in the corner showing horizontal ladder I/O device 310 and vertical ladder I/O device 320. The changing of direction can lead to small asymmetries in the device that in turn lead to skews in timing. **Figure 14** shows the waffle transistor design of the invention wherein symmetric I/O devices are used in I/O circuits eliminating asymmetries in corners of the chip and therefore benefiting the timing margin.

By improving the drain width to capacitance ratio in accordance with the embodiments described above, the capacitance on, for example, an I/O pad is reduced for the same current drive capability. This reduction in capacitance leads to faster transition times and enhances bus performance (e.g., bus speed). Further, the four-fold symmetry of the waffle FET design, in particular, reduces effects due to orientation, leading to less skew in the timing of the circuit performance.

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a performance circuit occupying a first area of an integrated circuit substrate; and

a protection circuit coupled to the performance circuit and having a size commensurate with dissipating an amount of predetermined charge incident on the performance circuit and occupying a second area of an integrated circuit substrate separate from the first area.

2. The integrated circuit of claim 1, wherein the performance circuit is configured to one of accept and drive a signal external to the integrated circuit.

3. The integrated circuit of claim 1, wherein the protection circuit is a diode.

4. The integrated circuit of claim 1, wherein the protection circuit includes:

a diode comprised of a unit block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region;

a junction region of the integrated circuit substrate surrounding the doped region; and

a contact to the doped region.

5. The integrated circuit of claim 4, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a first concentration of a second dopant and the junction region separating the first doped region from the well, the diode comprising a third doped region in the well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.

6. The integrated circuit of claim 5, wherein the diode is comprised of a plurality of unit blocks, each of the plurality of unit blocks having a first doped region of a first dopant in a well of the substrate and a junction region separating each of the first doped regions from the well.

7. The integrated circuit of claim 6, wherein the third doped region surrounds the junction.

8. The integrated circuit of claim 1, wherein the performance circuit includes:

a unit transistor having a drain region comprised of a unit block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region;

a gate region of the integrated circuit substrate surrounding the drain region; and

a contact to the doped region.

9. The integrated circuit of claim 8, the doped region having a first dopant in a well of the substrate, the well being doped with a second dopant, the transistor comprising a source region having the first dopant in the well separated from the drain region by the gate.

10. The integrated circuit of claim 9, wherein the performance circuit includes a plurality of unit transistors.

11. A buffer comprising:

complimentary metal oxide semiconductor (CMOS) device occupying a first area of an integrated circuit substrate; and

a protection circuit including a diode coupled to the CMOS device and occupying a second area of an integrated circuit substrate separate from the first area, the diode having a size commensurate with dissipating an amount of predetermined charge incident on the performance circuit.

12. The buffer of claim 11, wherein the buffer is one of an input buffer, an output buffer, and an input/output buffer.

13. The buffer of claim 11, wherein the CMOS device includes a p-channel device and the diode is coupled to the p-channel device.

14. The buffer of claim 13, the diode including:

a diode comprised of a plurality of unit blocks, each of the plurality of unit blocks having a p-doped region in an n-well of the substrate and occupying an area of the substrate sufficient to support a contact to the p-doped region;

a junction region separating each of the p-doped regions from the n-well; and

a contact to each of the plurality of unit blocks.

15. The buffer of claim 14, the diode further comprising an n-doped region adjacent the junction of each p-doped region, the n-doped region doped with a dopant concentration greater than a dopant concentration of the n-well.

16. The buffer of claim 15, wherein the n-doped region surrounds the junction.

17. The buffer of claim 11, wherein the CMOS device comprises:

a unit transistor having a drain region comprised of a unit block of a p-doped region in a well of the integrated circuit substrate, the unit block occupying an area of the substrate sufficient to support a contact to the p-doped region;

a gate region of the integrated circuit substrate surrounding the p-doped region; and

a contact to the p-doped region.

18. The buffer of claim 17, the well being doped with a first concentration of an n-type dopant, the unit transistor comprising a p-doped source region in the well separated from the drain region by the gate.

19. The buffer of claim 18, wherein the complimentary metal oxide semiconductor device comprises a plurality of unit transistors.

20. A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first area of an integrated circuit substrate;

forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area; and

coupling the protection circuit to the performance circuit.

21. The method of claim 20, wherein the step of forming a performance circuit includes a forming a CMOS device.

22. The method of claim 21, wherein the step of coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS device.

23. The method of claim 21, wherein the step of forming a protection circuit includes forming a diode and the step of

coupling the protection circuit to the performance circuit includes coupling the diode to the p-channel device of the CMOS.

24. The method of claim 20, wherein the step of forming a protection circuit includes forming a unit diode, the unit diode comprised of a block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region, a junction region of the integrated circuit substrate surrounding the doped region, and a contact to the doped region.

25. The method of claim 20, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a first concentration of a second dopant and the junction region separating the first doped region from the well, wherein the step of forming a protection circuit includes forming a third doped region in the well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.

26. The method of claim 25, wherein the step of forming a protection circuit includes forming a plurality of unit diodes.

27. The method of claim 20, wherein the step of forming a performance circuit includes:

forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate

occupying an area sufficient to support a contact to the doped region;

forming a gate region of the integrated circuit substrate surrounding the doped region; and

forming a contact to the doped region.

28. The method of claim 27, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a concentration of a second dopant and the step of forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor.

29. The method of claim 28, wherein the step of forming a performance circuit includes:

forming a plurality of unit transistors.

ABSTRACT OF THE INVENTION

An integrated circuit including a performance circuit occupying a first area of an integrated circuit substrate and a protection circuit coupled to the performance circuit and occupying a second area of an integrated circuit substrate separate from the first area. Also, a method of forming an integrated circuit including the steps of: Forming a performance circuit occupying a first area of an integrated circuit substrate, forming a protection circuit occupying a second area of an integrated circuit separate from the first area, and coupling the protection circuit to the performance circuit.

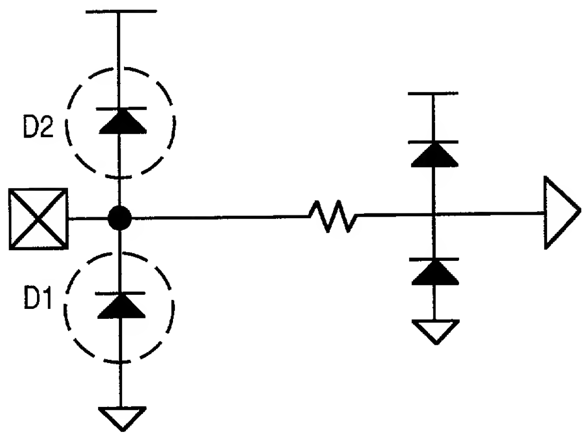


Fig. 1a
(Prior Art)

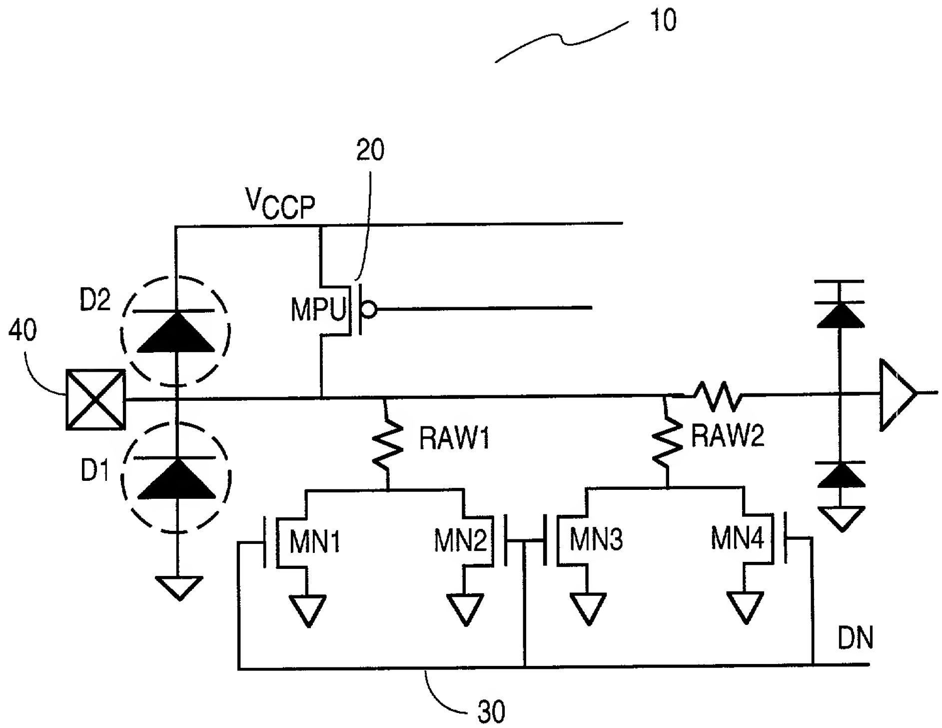


Fig. 1b
(Prior Art)

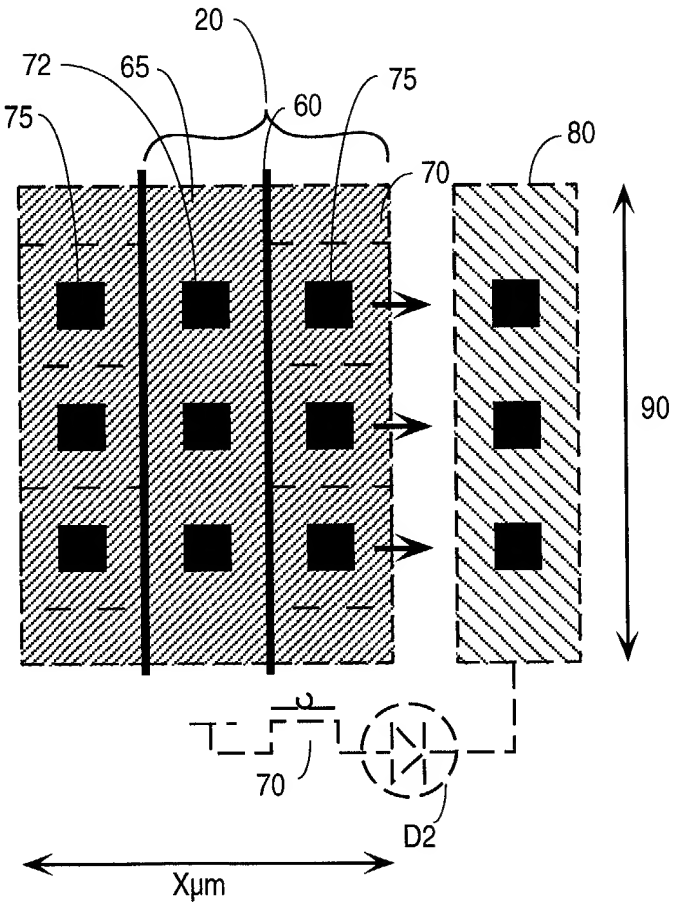


Fig. 2
(Prior Art)

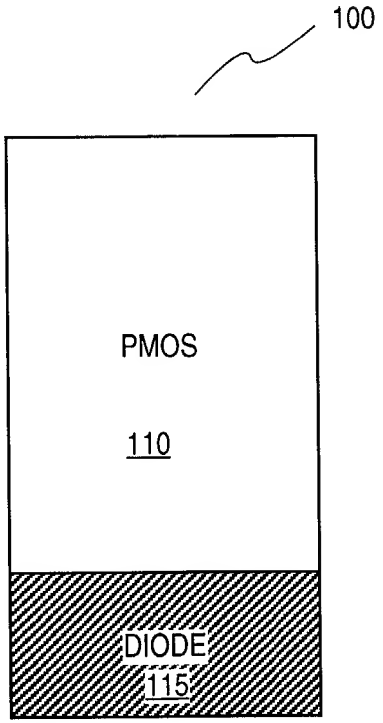
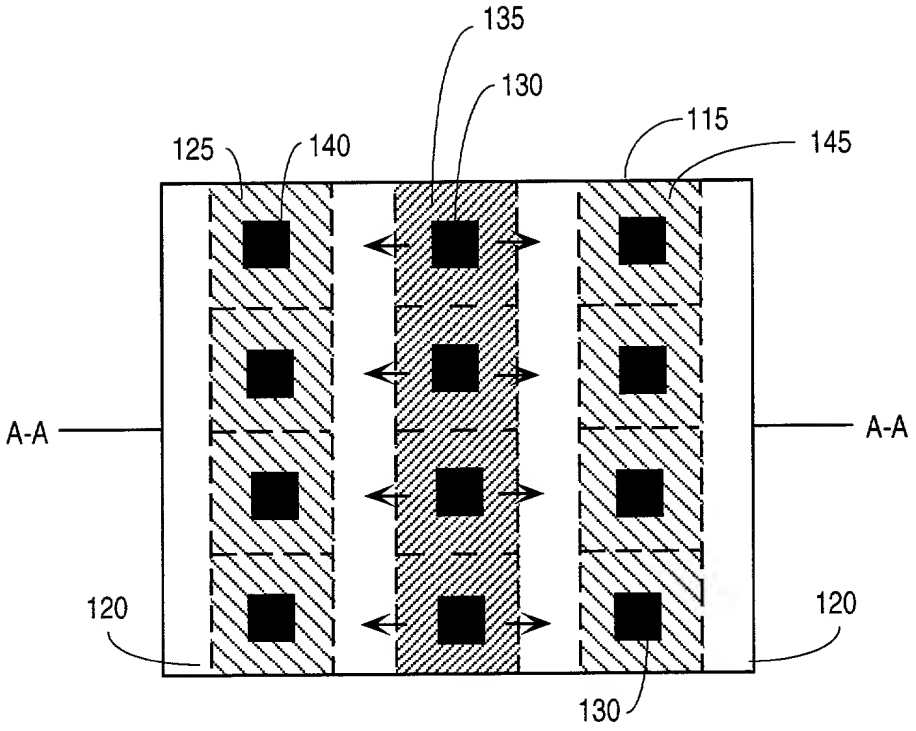


Fig. 3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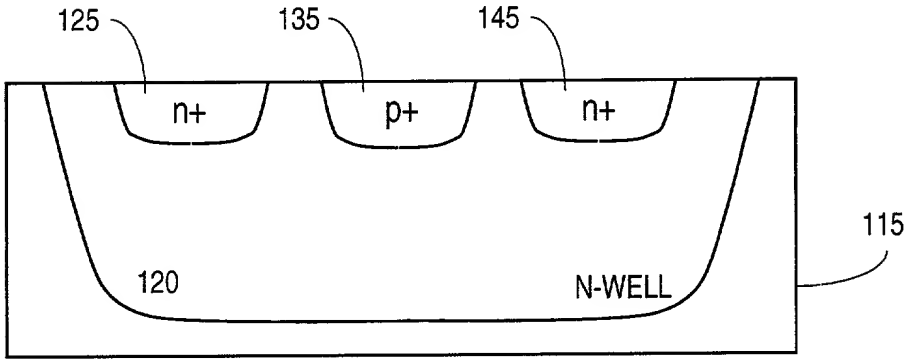
140
115
145
A-A
A-A
120
120
130

Fig. 4


125
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145
n+
p+
n+
115
120
N-WELL

Fig. 5

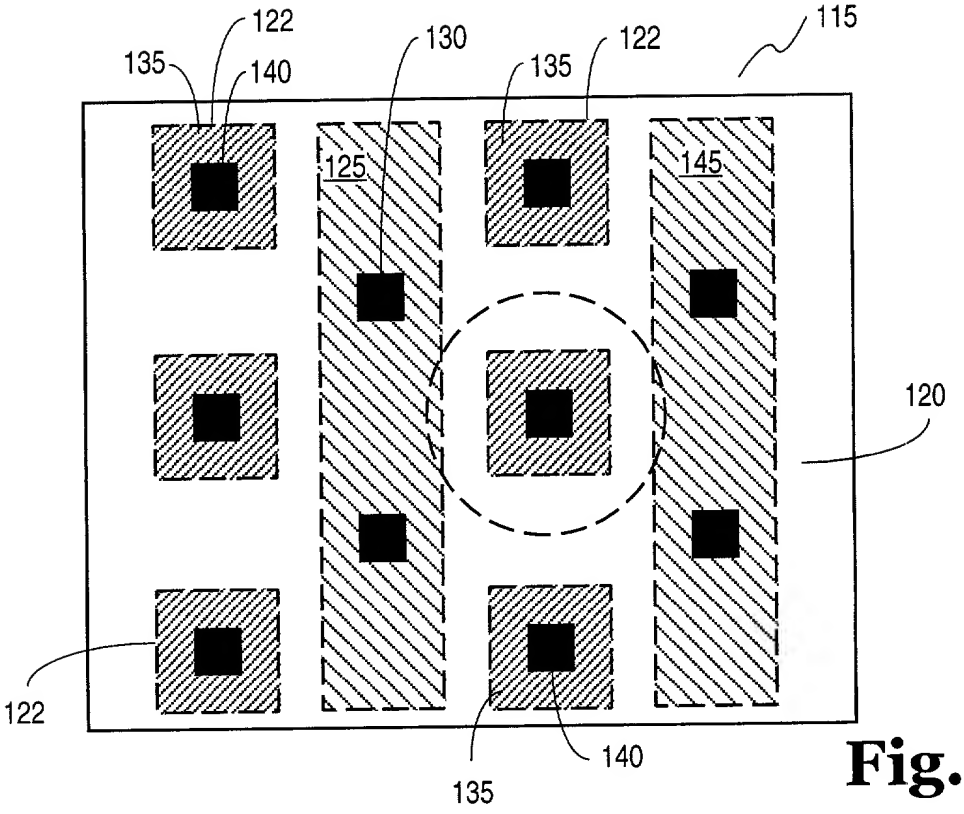


Fig. 6

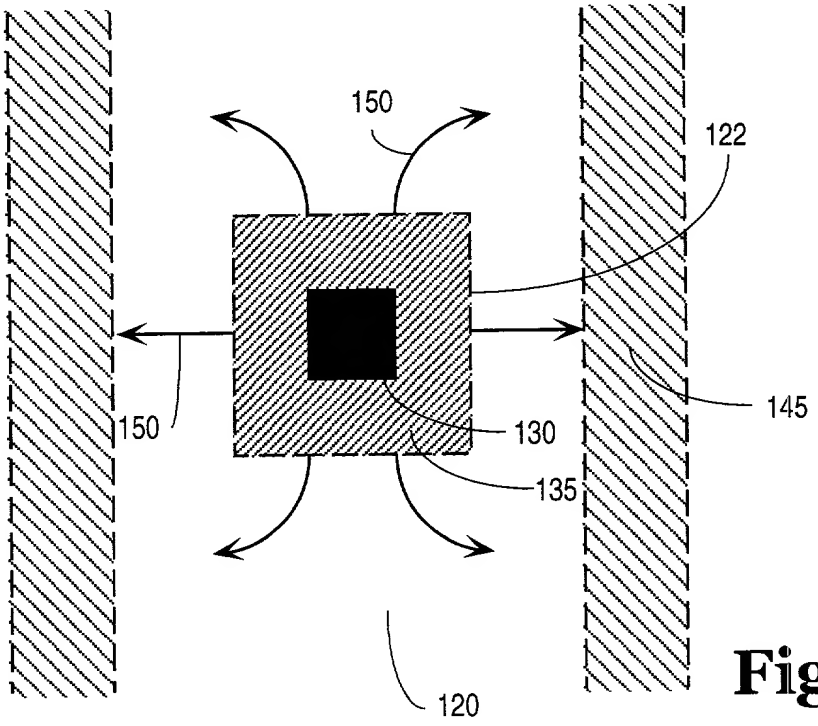


Fig. 7

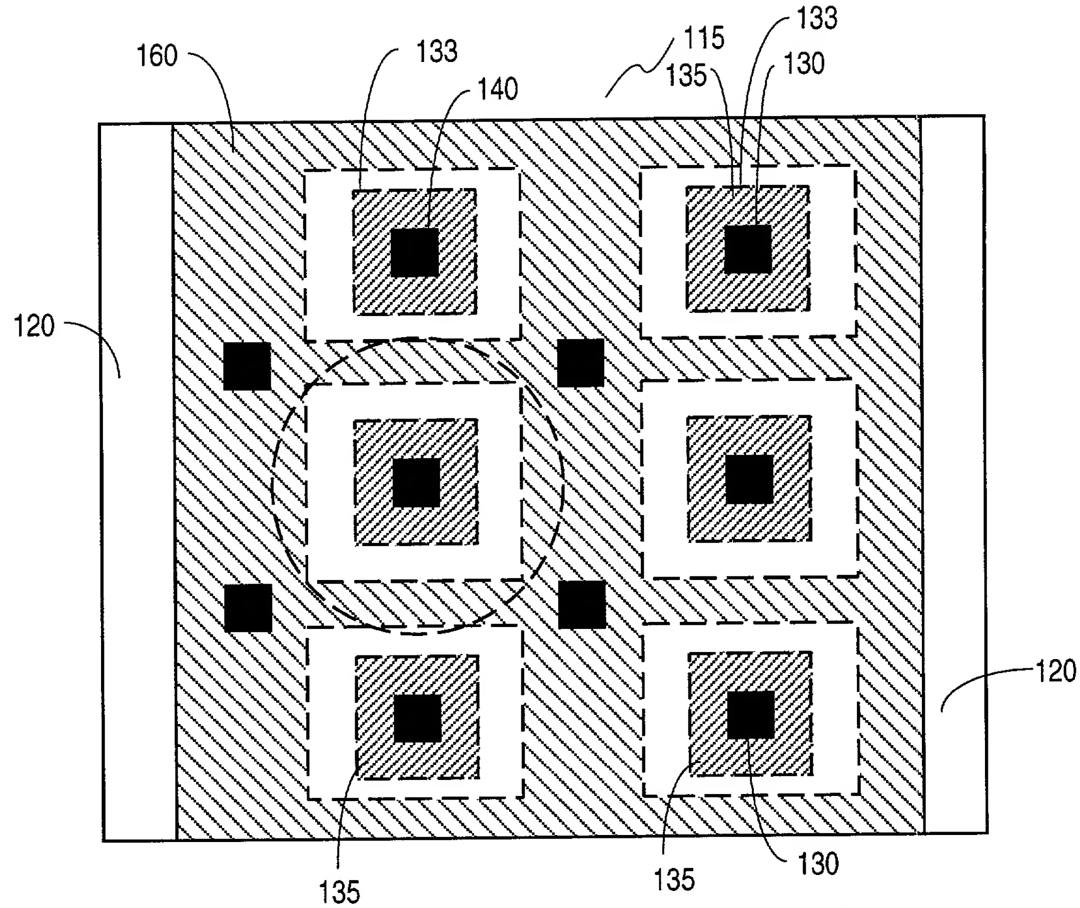


Fig. 8

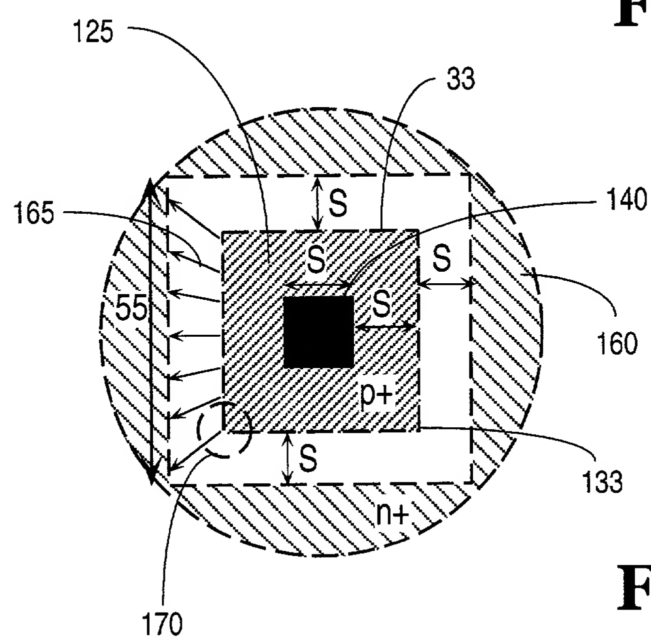


Fig. 9

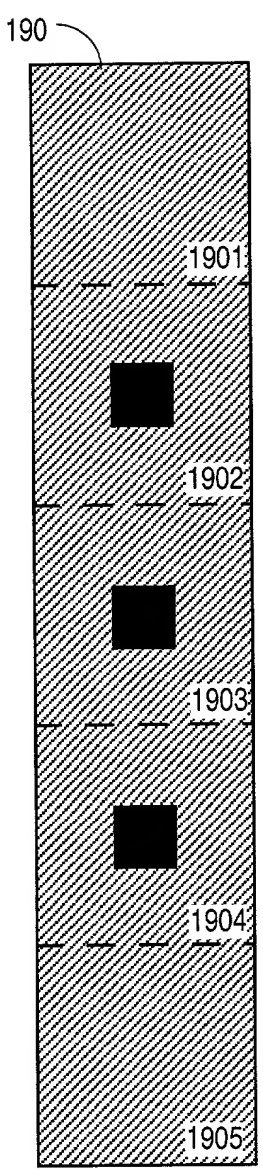


Fig. 10a
(Prior Art)

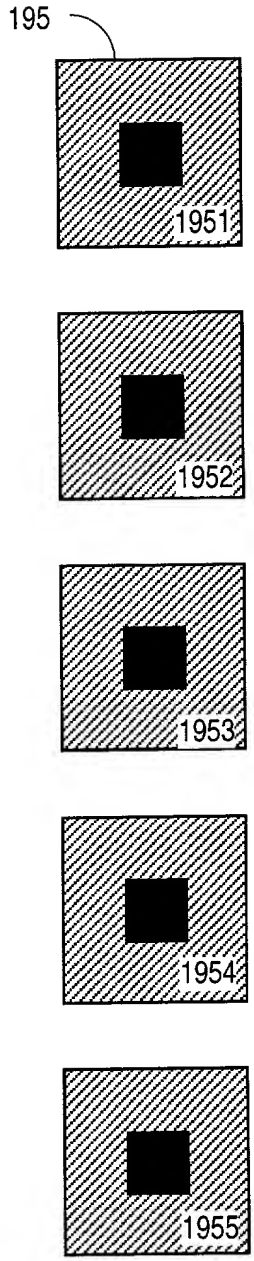
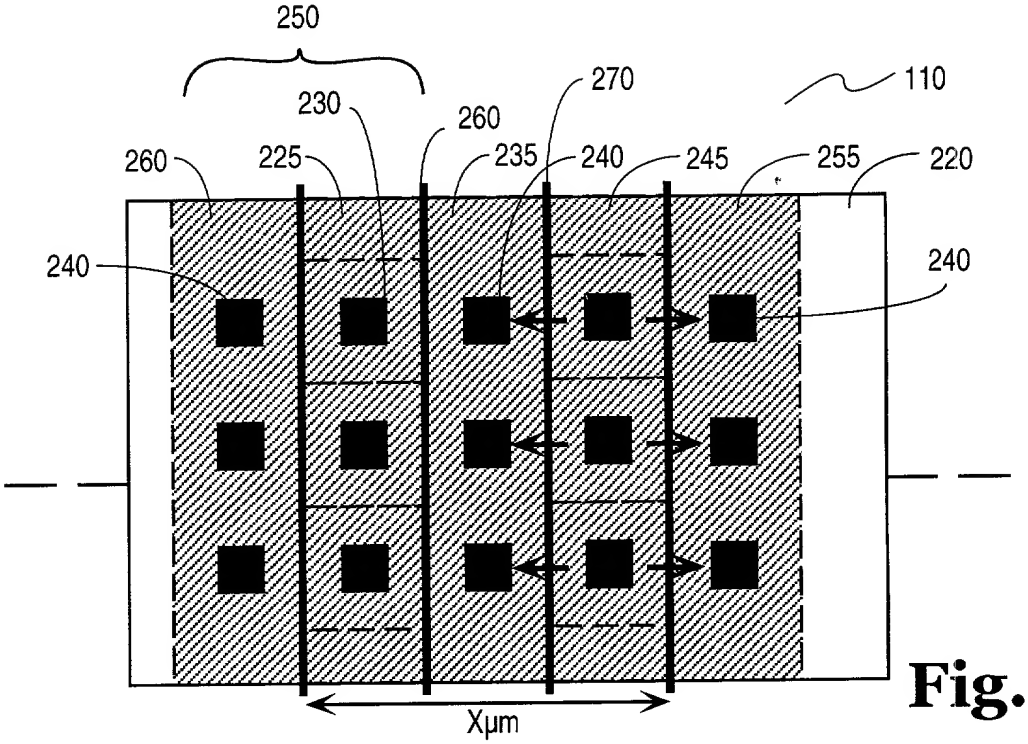


Fig. 10b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270
110
260
260
225
235
240
245
255
220
240
240
Xμm

Fig. 11

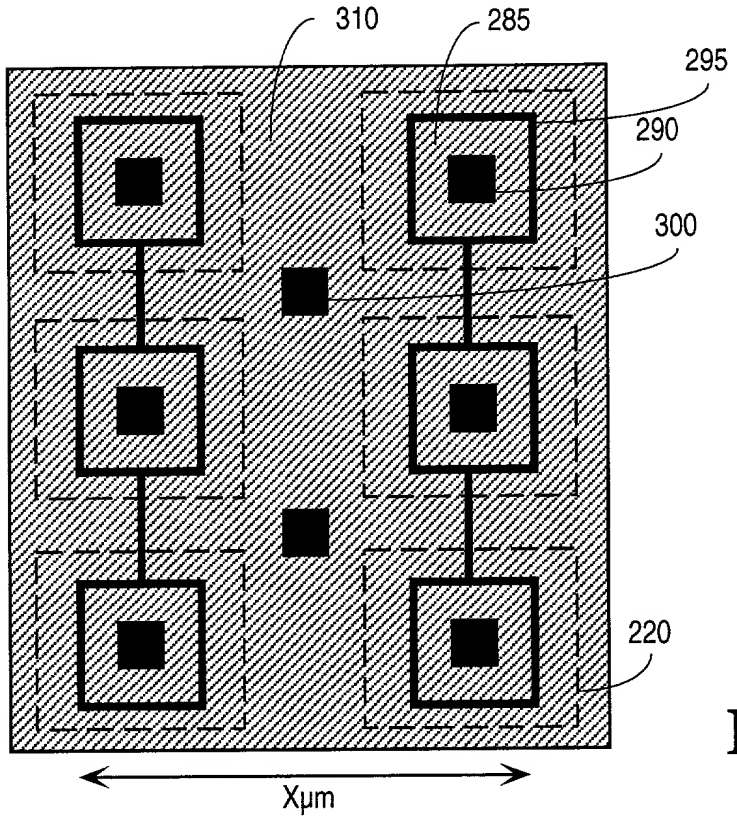
310
285
295
290
300
220
Xμm

Fig. 12

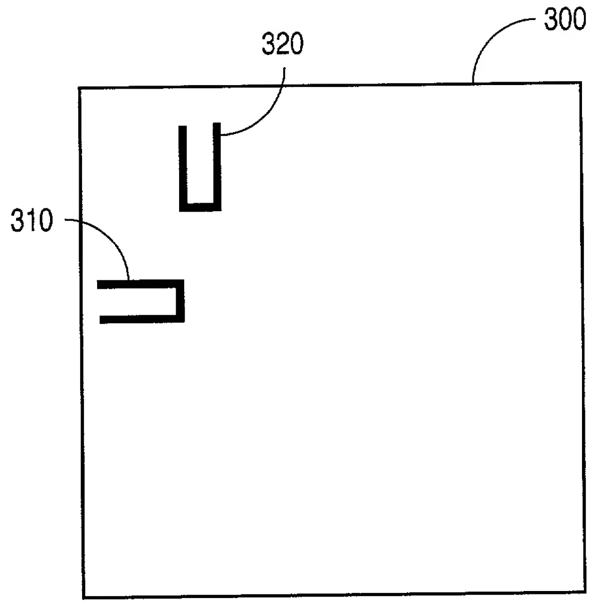

Fig. 13
(Prior Art)

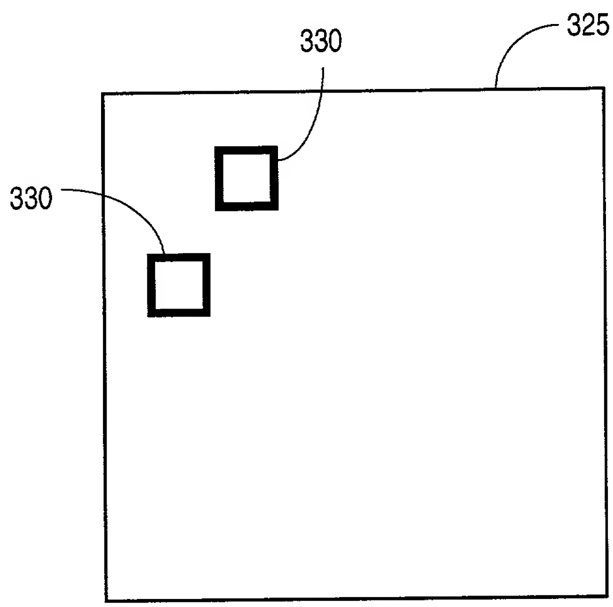

Fig. 14

Attorney's Docket No.: 042390.P5258

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Diode and Transistor Design for High Speed I/O

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Sharmini Nathan Green, Reg. No. 41,410; David R. Halvorson, Reg. No. 33,395; Eric Ho, Reg. No. 39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Judith A. Szepesi, Reg. No. 39,393; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Robert Andrew Diehl, Reg. No. 40,992; Thomas A. Hassing, Reg. No. 36,159; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewit

Send correspondence to William Thomas Babbitt, Reg. No. 39,591, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to William Thomas Babbitt, Reg. No. 39,591, (310) 207-3800.
(Name of Attorney or Agent)
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

P. O. Address _____

_____

Full Name of Fourth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

P. O. Address _____

_____

Full Name of Fifth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

P. O. Address _____

_____